ABSTRACT OF THE DISCLOSURE

Level control signals are both set to H level, and potentials of power supply lines are both set to be lower than a power supply potential. In this manner, a gate leakage current during waiting and writing operation of a memory cell array can significantly be reduced. The level control signals are set to L level and H level respectively, and solely the potential of one of the power supply lines is set to be lower than the power supply potential. In this manner, power consumption during a reading operation of the memory cell array can be reduced.